REMARKS

I. STATUS OF CLAIMS

In accordance with 37 C.F.R. § 1.173(c), the status of the claims are as follows:

Claims 1-33 and 40-54 are pending in the reissue application.

Claims 1-33 are original claims and remain allowed. No changes have been made to claims 1-33.

Claims 34-54 were previously added in the preliminary amendment filed November 24, 2003, with claims 34-39 being canceled in the previous amendment filed November 20, 2006.

No amendments are being made in this response.

II. PRIOR ART REJECTION

Claims 34-54 stand rejected under 35 U.S.C. § 102 as being anticipated by Eickemeyer et al. '746 ("Eickemeyer"). Claims 40 and 47 are independent. This rejection is respectfully traversed for the following reasons.

Claims 40 and 47 each embody an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the bit width of the instruction bus is shorter than M * N bits; where M is the maximum bit length of an instruction that can be executed in parallel and N is the number of instructions that can be executed in parallel. In direct contrast, Eickemeyer expressly discloses (col. 12, lines 5-14):

> the rule for compounding a set of instructions which includes variable instruction lengths provides that all instructions which are 2 bytes or 4 bytes long are compoundable with each other. That is, ... a 4 byte instruction is capable of parallel execution with another 2 byte ***or another 4 byte instruction***. The rule further provides that all instructions which are 6 bytes long are not compoundable. (emphasis added)

Accordingly, Eickemeyer discloses only a conventional bus configuration having a bus width which is sufficient to handle processing the maximum bit size.

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Pan. Applicants and Applicants' representative would like to thank Examiner Pan for his courtesy in conducting the interview and for his assistance in resolving issues. A summary of the interview discussion follows.

As previously mentioned, the maximum bit length of an instruction that is executed in parallel in Eickemeyer is 4 bits so that M = 4 (though Eickemeyer references "bytes," because the analysis does not change, they are being equated to "bits" throughout this discussion for simplicity). Further, the number of instructions which are executed in parallel is 2 so that N = 2. During the interview, the Examiner alleged that the term "maximum" as used where M is the maximum bit length of an instruction that can be executed in parallel, could be interpreted broadly onto the device of Eickemeyer for the disclosed condition in Eickemeyer when a 4 bit instruction is executed in parallel with a 2 bit. Accordingly, the Examiner concluded that the bit width of the instruction bus for such a condition would be 4 + 2 = 6 so as to be shorter than M * N bits (4 * 2 = 8).

However, as explained during the interview and as would understood by one of ordinary skill in the art, the bit width of the instruction bus is a structural parameter defining the available space in the instruction bus. Accordingly, because Eickemeyer expressly discloses that a 4 "bit" instruction is capable of parallel execution with another 4 bit instruction, the bit width of the instruction bus of Eickemeyer must be at least 8 bits to accommodate the two 4 "bit" instructions. The Examiner can not interpret the condition in which the instruction bus is not accessed for its entire width (e.g., when a 2 bit and 4 bit instruction are processed) as definitive

of the actual bit width of the instructions bus. In this regard, to emphasize this point, the following analogy is provided: a three-lane highway is still a three-lane highway even if only one lane is being used by drivers at a particular point in time. Similarly, the instruction bus of Eickemeyer is an 8 bit "highway" even if during a given processing sequence only 6 bits are being used. Accordingly, the bit width of the instruction bus in Eickemeyer is at least equal to (M * N) 4 * 2 = 8 bits so as to accommodate the expressly disclosed capability of having two 4 bit instructions processed in parallel, so that the bit width of the instruction bus in Eickemeyer is NOT shorter than M * N bits.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Eickemeyer does not anticipate claims 40 and 47, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 40 and 47 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

III. CONCLUSION

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
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